WEST BENGAL STATE UNIVERSITY

B.Sc. Honours 3rd Semester Examination, 2019

PHSACOR07T-PHYSICS (CC7)

DIGITAL SYSTEMS AND APPLICATIONS

Time Allotted: 2 Hours | Full Marks: 40

The figures in the margin indicate full marks.
Candidates should answer in their own words and adhere to the word limit as practicable.
All symbols are of usual significance.

Answer Question No. 1 and any *two* from the rest

1. Answer any ***ten*** questions: $2\times10 = 20$

   (a) What are active and passive electronic components? Give examples.

   (b) Why a time base signal is used in a CRO?

   (c) Subtract $(1011)_2$ from $(11011)_2$ by 2'S complement method.

   (d) Convert $(DB19)_{16}$ to octal number.

   (e) What do you mean by minterms and maxterms?

   (f) Draw functional block diagram of a 555 timer IC.

   (g) Prove using boolean logic the identity

   $$\overline{A} + \overline{AB} + AB = 1$$

   (h) Design a 1:2 Demultiplexer.

   (i) Draw the block diagram of 3-bit synchronous counter.

   (j) What is the function of an encoder?

   (k) What is the difference between RAM and ROM?

   (l) What is the difference between latch and flip flop?

   (m) Classify registers in respect of operation.

   (n) Draw a circuit of parity checker using logic gates.

2. (a) Give the block diagram of a general purpose CRO. How can the phase difference between two AC voltages be measured using CRO? 2+2

   (b) An unknown sinusoidal voltage is displayed on the CRO screen. If the peak to peak distance of the displayed waveform is 8 divisions of the vertical scale and V/div control is set at 5 mV/div. Find the r.m.s value of a.c. voltage. 3

   (c) Draw a circuit of 4:1 multiplexer, give its logic equation and truth table. 3

3. (a) Given the truth table. 1+2 +1

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

(i) Find the logic equation.

(ii) Simplify it using Karnaugh map.

(iii) Draw the simplified logic circuit.

(b) Show that a NAND-NAND configuration is equivalent to a AND-OR configuration. 2

(c) Draw an ADDER circuit using logic gates. 2

(d) Draw the circuit of a NAND gate using discrete components. 2

4. (a) Draw the circuit diagram of a J-K flip flop. Give its truth table and explain race-around condition. 1+1+2

(b) Draw the circuit diagram of a D-type and T-type flip flop using J-K flip flop. 1+1

(c) Draw the circuit diagram of an astable multivibrator using 555 timer. 2

(d) What is edge triggering? Explain. 2

5. (a) Construct a 4-bit shift register using J-K flip flop. Write down a table of the readings of the shift register after each clock pulse by assuming the data '1011'. 2+2

(b) Explain with the help of relevant circuit diagram the operation of decade counter. 2+2

(c) Show the timing diagram of a 3-bit synchronous counter. 2

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