WEST BENGAL STATE UNIVERSITY

B.Sc. Honours 3rd Semester Examination, 2019

ELSACOR06T-ELECTRONICS (CC6)

Time Allotted: 2 Hours | Full Marks: 40

The figures in the margin indicate full marks.
Candidates should answer in their own words and adhere to the word limit as practicable.
All symbols are of usual significance.

GROUP-A

1. Answer any ***five*** questions from the following: 2×5 = 10

   (a) How can a decoder be used as a demultiplexer?

   (b) Subtract $(1001)_2$ from $(1100)_2$ using the 1's complement method.

   (c) What is priority encoder?

   (d) Design a three input NAND gate using two input NAND gates and write down its truth table.

   (e) What do VHDL stands for? Write the advantages of VHDL.

   (f) Write syntax of process statement used in VHDL and in which type of modeling style it is used.

   (g) What is the difference between concurrent and sequential statements?

   (h) Write the name of various types of delays in VHDL.

   (i) Cascade two 4:1 Mux Ic's (74151) to make 8:1 Mux.

   (j) Distinguish between binary and BCD codes.

GROUP-B

Answer any *six* questions from the following 5×6 = 30

2. Explain half-adder with neat logic diagram and truth table. 5

3. Explain the action of 2-input TTL NAND gate with neat diagram. 5

4. (a) Prove that Multiplexer is an Universal Logic Module. 3

   (b) What is the role of don't care condition in simplification of Boolean expressions using Karnaugh Map? 2

5. (a) Minimize the following function using K-map 3

$$F(A, B, C, D) = \sum(1, 3, 5, 7, 9, 10, 12, 13)$$

(b) What is shift register? 2

6. Explain clocked S-R Flip-Flop with neat diagram and truth table. 5

7. Draw the logic diagram for four bit ring counter and explain it. 5

8. (a) Implement the following function using 8:1 Mux. 3

$$F = \sum(0, 1, 3, 5, 10, 11, 13, 15)$$

(b) What is race around condition? 2

9. Distinguish between: $2\frac{1}{2}+2\frac{1}{2}$

(i) VHDL IF and VHDL case

(ii) VHDL Next and Exit.

10. Explain the implementation of single dimensional and two dimensional arrays in VHDL. How the race around condition be overcome? $3\frac{1}{2}+1\frac{1}{2}$

11.(a) What is the difference between combinational and sequential logic circuits? 2

(b) Draw a neat circuit of a 4-bit Adder | Subtractor. 3

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